Appl. No. 10/815,201

Attorney Docket No.: N1280-00180 (TSMC2003-1083)

Reply dated: 09/19/2006

Supplemental Response to Office Action dated 04/20/2006

and Advisory Action dated 08/25/2006

## Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application.

- 1 1. (Cancelled)
- 1 2. (Cancelled)
- 1 3. (Cancelled)
- 1 4. (Cancelled)
- 1 5. (Cancelled)
- 1 6. (Cancelled)
- 1 7. (Cancelled)
- 1 8. (Currently Amended) An SRAM cell formed on an insulator substrate, the cell
- 2 comprising:
- at least one active region formed on the insulator substrate and
- 4 with a continuous silicide layer formed thereon serving as an intra-cell connection layer
- 5 connecting at least a drain node[[s]] of at least a PMOS transistor to a drain node of and
- 6 an NMOS transistor formed on the insulator substrate, the two transistors forming a first
- 7 inverter;
- 8 said continuous silicide layer further forming a sidewall butted
- 9 connection structure used in conjunction with a gate interconnect layer and connecting
- 10 the drain nodes of the transistors of the first inverter to gates of at least two transistors
- 11 of a second inverter.

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- wherein the continuous silicide layer consists of a first silicide film formed
- 13 of silicon from the active region and a second silicide film formed of silicon from the gate
- 14 interconnect layer.
- 1 9. (Original) The cell of claim 8 wherein the active region further connects to a
- 2 source node of at least one pass gate.
- 1 10. (Original) The cell of claim 9 wherein the pass gate's drain node is connected to
- 2 an access line.
- 1 11. (Original) The cell of claim 8 further comprising a first metal layer for forming
- 2 wordline metal straps and landing pads for power supply lines and access lines.
- 1 12. (Original) The cell of claim 11 further comprising a second metal layer for forming
- 2 power supply lines and access lines.
- 1 13. (Original) The cell of claim 12 wherein the access lines are interposed between
- 2 the power supply lines.
- 1 14. (Original) The cell of claim 11 wherein lines on the first and second metal layers
- 2 are arranged in a substantially perpendicular fashion.
- 1 15. (Previously Presented) An SRAM cell formed on an insulator substrate, the cell
- 2 comprising:
- a first inverter having a first PMOS transistor and a first NMOS
- 4 transistor;
- 5 a second inverter having a second PMOS transistor and a second
- 6 NMOS transistor; and
- 7 a sidewall butted connection structure used in conjunction with a
- 8 gate interconnect layer for connecting drain nodes of the transistors of the first inverter

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- 9 formed on an active region disposed on the insulator substrate, to gates of the two
- 10 transistors of the second inverter,
- wherein the sidewall butted connection structure is a continuous silicide
- 12 layer including a junction covering a dielectric edge portion between the active region
- and the gates of the two transistors and consists of a first silicide film formed of silicon
- 14 from the single-crystal active region and a second silicide film formed of silicon from the
- 15 gates.
- 1 16. (Original) The cell of claim 15 further comprising a first metal layer for forming
- 2 landing pads for at least one wordline and at least one power supply line or access line.
- 1 17. (Original) The cell of claim 15 wherein the first metal layer is also used for
- 2 forming a connection between the drain nodes of the two transistors of the first or
- 3 second inverter.
- 1 18. (Original) The cell of claim 16 further comprising a second metal layer for forming
- 2 at least one wordline metal strap and landing pads for at least one power supply line or
- 3 access line.
- 1 19. (Original) The cell of claim 18 further comprising a third metal layer for forming
- 2 power supply lines and access lines.
- 1 20. (Original) The cell of claim 19 wherein the access lines are interposed between
- 2 the power supply lines.
- 1 21. (Original) The cell of claim 15 further comprising at least one active region with a
- 2 silicide layer formed thereon serving as an intra-cell connection layer connecting drain
- 3 nodes of the transistors of the first inverter.

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- 1 22. (Original) The cell of claim 15 wherein the sidewall butted connection structure is
- 2 electrically connected to a source node of a pass gate.
- 1 23. (Original) The cell of claim 15 further comprising a first metal layer for forming at
- 2 least one power supply line and at least one access line.
- 1 24. (Original) The cell of claim 23 further wherein the first metal layer is used for
- 2 forming landing pads for at least one wordline, or landing pads for at least one power
- 3 supply line.
- 1 25. (Original) The cell of claim 23 further comprising a second metal layer for forming
- 2 at least one wordline metal strap and at least one power supply line.
- 1 26. (Cancelled)
- 1 27. (Cancelled)
- 1 28. (Cancelled)
- 1 29. (Cancelled)
- 1 30. (Cancelled)
- 1 31. (Cancelled)